## REMARKS

Claims 2 and 15 have been canceled, Claims 1, 3, 4, 9, 14 and 16 have been amended, Claim 20 has been added, and Claims 1, 3-14 and 16-19 are pending in this application. Reconsideration of this application is respectfully requested.

Minor typographical errors were uncovered during review of the specification, which have been corrected.

The Abstract was objected to because it exceeds 150 words. The Abstract has been amended to recite less than 150 words. The Abstract has been amended to contain 143 words. Withdrawal of the Examiner's objection is respectfully requested.

Claims 3, 4, 9 and 16 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Examiner pointed out certain antecedent basis and clarity issues in these Claims. Claims 3, 4, 9 and 16 have been amended to address the Examiner's issues and are believed to be clear and definite. In view of these amendments, withdrawal of the Examiner's rejection is respectfully requested.

Claims 1, 3-6, 8, 10, 11, 13, 14, 16, 17 and 19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent No. 6,378,104 issued to Okita in view of US Patent No. 6,317,858 issued to Cameron. The essence of the Examiner's rejection is that the Okita patent substantially discloses the present invention as recited in Claim 1, but fails to "explicitly teach the specific use of a Chien-Forney module using Forney algorithms to calculate error values." The Cameron patent is cited as disclosing "using Forney algorithms to calculate error values (Forney algorithm circuit 15 in Cameron)."

The Examiner indicated that "One of ordinary skill in the art at the time the invention was made would have been highly motivated to combine the teachings of the Okita patent with the teachings in the Cameron patent since the error correction system in the Okita patent requires a means for determining error values and Forney's algorithm is a well-known means, that one of ordinary skill would have been apprised of, for determining error values." However, it is respectfully submitted that amended Claim 1 is patentable over the combined teachings of the Okita and Cameron patents, taken singly or together, or any of the other cited patents taken in combination with the Okita and Cameron patents.

The Okita patent states at column 2, lines 39-46 that "The RS decoding device usually comprises a syndrome operation circuit, error-position polynomial and evaluating polynomial operation circuit, error-position detector, evaluation value detector, and correction execution circuit. Among these, for the aforementioned error-position polynomial operation circuit and evaluating polynomial operation circuit, the Euclid and the Berlekamp-Massey algorithm are known algorithms."

Claim 1 calls for "a translator circuit ... for translating the external Galois-field representation of the received code into an internal Galois-field representation comprising a quadratic-subfield representation of the code" and "an inverse translator circuit for translating

the internal quadratic-subfield Galois-field representation of the error-corrected code into the external Galois-field representation." It is respectfully submitted that the Okita or Cameron patents, taken singly or together, do not disclose or suggest these aspects recited in Claim 1.

It is respectfully submitted that neither the Okita or Cameron patents, taken singly or together, or taken in combination with any of the other cited patents, do not disclose or suggest the use of internal quadratic-subfield Galois-field representations of codes. It is respectfully submitted that neither the Examiner's assertion with regard to the rejection of Claims 2 and 15 that " the Input-Side Transformation Circuits 116 is a translator for translating data from one Galois Field to another" is not a disclosure or suggestion regarding translation to a quadratic-subfield Galois-field representation as is presently claimed. The terms "quadratic", "subfield" or "quadratic-subfield" are not used in the Okita or Cameron patents. It is respectfully submitted that the Examiner's assertions are not supported by the teachings of the Okita or Cameron patents.

In view of the above, it is respectfully submitted that Claim 1 is not obvious in view of the Okita or Cameron patents, taken singly or together. Withdrawal of the Examiner's rejection and allowance of Claim 1 are respectfully requested.

With regard to Claim 14, and in view of the arguments made with respect to Claim 1, it is respectfully submitted that the Okita or Cameron patents, taken singly or together, do not disclose or suggest "translating one of a predetermined number of Reed-Solomon and BCH codes that each have predetermined external Galois-field representations into an internal quadratic subfield Galois-field representation" or "translating the internal quadratic subfield Galois-field representation of the error-corrected code into the external Galois-field representation". Neither of the cited patents disclose or suggest a method for decoding Reed-Solomon and BCH codes using quadratic subfield Galois-field representations of the codes. The terms "quadratic", "subfield" or "quadratic-subfield" are not used in the Okita or Cameron patents or any of the other cited patents for that matter.

Therefore, it is respectfully submitted that Claim 14 is not obvious in view of the Okita or Cameron patents, taken singly or together. Withdrawal of the Examiner's rejection and allowance of Claim 14 are respectfully requested.

Dependent Claims 3-6, 8, 10, 11, 13, 16, 17 and 19 are considered patentable based upon the allowability of Claims 1 and 14 from which they depend.

With regard to Claim 3, is respectfully submitted that the Okita or Cameron patents, taken singly or together, do not disclose or suggest the use of a Berlekamp-Massey module that "carries out repeated dot product calculations between vectors" The terms "dot product" and "repeated dot product calculations" are not used in the Okita or Cameron patents.

With regard to Claim 4, and in view of the arguments made with regard to Claim 1, it is respectfully submitted that the Okita or Cameron patents, taken singly or together, do not disclose or suggest the use of "quadratic-subfield modular multipliers". It is respectfully submitted that the Examiner's position is not supported by the express teachings of the cited

patents and amount to hindsight reconstruction of the present invention.

With regard to Claim 5, and in view of the arguments made with regard to Claim 1, it is respectfully submitted that the Okita or Cameron patents, taken singly or together, do not disclose or suggest that "the Berlekamp-Massey computation module and the Chien-Forney module each include a quadratic-subfield-power integrated divider that carries out Galois-field division in a quadratic-subfield representation". It is respectfully submitted that the Examiner's assertion regarding the Okita patent is not a disclosure or suggestion of a quadratic-subfield-power integrated divider that is specifically recited in Claim 5.

With regard to Claim 8, is respectfully submitted that the use of a switch referred to by the Examiner is not a disclosure or suggestion regarding "providing for switching among different codes and among codes of different degrees of shortening." This is not discussed in either the Okita or Cameron patents.

With regard to Claim 16, is respectfully submitted that the Okita or Cameron patents, taken singly or together, do not disclose or suggest the use of a Berlekamp-Massey module that "carries out repeated dot product calculations between vectors" The terms "dot product" and "repeated dot product calculations" are not used in the Okita or Cameron patents.

In view of the above, it is respectfully submitted that Claims 3-6, 8, 10, 11, 13, 16, 17 and 19 are not obvious in view of the Okita or Cameron patents, taken singly or together. Withdrawal of the Examiner's rejection and allowance of Claims 3-6, 8, 10, 11, 13, 16, 17 and 19 are respectfully requested.

Claim 7 was rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent No. 6,378,104 issued to Okita and US Patent No. 6,317,858 issued to Cameron in view of US Patent No. 5,323,402 issued to Vaccaro et al. The Examiner admitted that "Okita and Cameron does not explicitly teach the specific use of a systolic decoder." The Examiner stated that "Vaccaro, in an analogous art, teaches a systolic decoder.", and concluded that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Okita and Cameron with the teachings of Vaccaro by including use of a systolic decoder."

Claim 7 recites that "clocks controlling the syndrome computation module, the Berlekamp-Massey computation module, and the Chien-Forney module are separate and free-running clocks requiring no fixed phase relationship, to allow maximum speed and flexibility for the clocks of each module." It is respectfully submitted that there is no disclosure contained in the Okita, Cameron or Vaccaro et al. patents, taken singly or together, that suggests this. The mere fact that the Vaccaro et al. patent states that it is a "programmable systolic BCH decoder" (see title) is not a disclosure or suggestion of the aspects of the present invention specifically recited in Claim 7. It is respectfully submitted that there is no disclosure or suggestion in the Vaccaro et al. patent regarding the use of "free-running clocks" or "free-running clocks requiring no fixed phase relationship" as is recited in Claim 7. The term "free-running clock" is not used in any of the cited patents.

It is respectfully submitted that there is no specific teaching contained in the Okita, Cameron or Vaccaro et al. patents which would provide for combining them, absent hindsight reconstruction on the part of the Examiner.

It is also respectfully submitted that Claim 7 is patentable based upon the allowability of Claim 1 from which it depends. Accordingly, it is respectfully submitted that Claim 7 is not obvious in view of the Okita, Cameron or Vaccaro et al. patents, taken singly or together. Withdrawal of the Examiner's rejection and allowance of Claim 7 are respectfully requested.

Claim 9 was rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent No. 6,378,104 issued to Okita and US Patent No. 6,317,858 issued to Cameron in view of US Patent No. 5,754,563 issued to White. The Examiner admitted that "Okita and Cameron does not explicitly teach the specific use of dual mode operations." However, the Examiner stated that "White, in an analogous art, teaches N channels for parallel processing N blocks of encoded data." The Examiner concluded that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Okita and Cameron with the teachings of White by including use of dual mode operations."

It is respectfully submitted that the Okita and Cameron devices would not be modified in light of the teachings of the White patent without using hindsight reconstruction. There is disclosure or suggestion contained in the Okita or Cameron patents regarding the desire to process data in parallel, and therefore adding this feature was not contemplated by them. Modifying the teachings of the Okita or Cameron patents to provide for parallel operation therefore extends their express teachings beyond the scope of the patents, using hindsight reconstruction, using the teachings of the cited patents in light of Applicants' own teachings.

It is also respectfully submitted that Claim 9 is patentable based upon the allowability of Claim 1 from which it depends. Accordingly, it is respectfully submitted that Claim 9 is not obvious in view of the Okita, Cameron or White patents, taken singly or together. Withdrawal of the Examiner's rejection and allowance of Claim 9 are respectfully requested.

Claims 12 and 18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent No. 6,378,104 issued to Okita and US Patent No. 6,317,858 issued to Cameron in view of US Patent No. 5,323,402 issued to Vaccaro et al. The Examiner admitted that "Okita and Cameron does not explicitly teach the specific use of a systolic decoder." However, the Examiner stated that "Vaccaro, in an analogous art, teaches a systolic decoder." The Examiner concluded that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Okita and Cameron with the teachings of Vaccaro by including use of a systolic decoder."

It is respectfully submitted that a review of the Vaccaro et al. patent reveals that it does not disclose or suggest "exclusive-OR trees" used in the "syndrome module and the Chien-Forney module." In fact, the Vaccaro et al. patent does not even refer to "exclusive-OR trees" or a "Chien-Forney module." The terms "exclusive-OR trees" and "Chien-Forney" are not even used in the Vaccaro et al. patent.

With regard to Claim 12, is respectfully submitted that the Okita, Cameron or Vaccaro et al. patents, taken singly or together, do not disclose or suggest that "alterations solely in exclusive-OR trees of the syndrome module and the Chien-Forney module enable the decoder to decode Reed-Solomon codes using code-generator polynomials having any offset and skip values, including standard code-generator polynomials."

With regard to Claim 12, is respectfully submitted that the Okita, Cameron or Vaccaro et al. patents, taken singly or together, do not disclose or suggest that "alterations solely in exclusive-OR trees enable decoding of Reed-Solomon codes using code-generator polynomials having any offset and skip values, including standard code-generator polynomials."

Dependent Claims 12 and 18 are also considered patentable based upon the allowability of Claims 1 and 14 from which they depend. Accordingly, it is respectfully submitted that Claims 12 and 18 are not obvious in view of the Okita, Cameron or Vaccaro et al. patents, taken singly or together. Withdrawal of the Examiner's rejection and allowance of Claims 12 and 18 are respectfully requested.

With regard to newly added Claim 20, is respectfully submitted that none f the cited references, taken singly or together, disclose or suggest an error correction decoder comprising "a translator circuit ... for translating the external Galois-field representation of the received code into an internal Galois-field representation comprising a quadratic-subfield representation of the code", "a Berlekamp-Massey computation module comprising quadratic-subfield multipliers that implements a Berlekamp-Massey algorithm that converts the syndromes to intermediate results comprising lambda and omega polynomials", and "an inverse translator circuit for translating the internal quadratic-subfield Galois-field representation of the error-corrected code into the external Galois-field representation."

It is stated in the specification in the paragraph starting at page 11, line 26, for example, that the present invention employs "novel and greatly improved Galois-field multipliers and divider modules that are made possible by the use of a quadratic-subfield representation on-chip." This is made possible by the translator and inverse translator circuits that translate from an external Galois-field representation to an internal quadratic-subfield Galois-field representation to an external Galois-field representation corresponding to the codes.

It is also stated in the specification at page 12, lines 19-28, for example, that "The Berlekamp-Massey module 15 carries out repeated dot product calculations between vectors with up to seventeen components using Galois-field arithmetic. The usual textbook method of doing this is to have a single multiplication circuit as part of a Galois-field arithmetic logic unit (GFALU). Instead, in the decoder 10, seventeen parallel multipliers implemented in the Berlekamp-Massey module 15 are used to carry out the dot product in one step. This massive parallelism significantly increases speed, and is made feasible because of the optimizing choice of an internal quadratic-subfield Galois-field representation that is different from the representation used off-chip. The parallel multiplier circuit operating in an internal quadratic-subfield Galois-field representation is a novel feature of the present invention."

The terms "quadratic", "subfield" or "quadratic-subfield" are not used in any of the cited patents. The Okita patent appears to disclose the use of a multiplier 113 that is a single multiplication circuit as is conventionally used, as mentioned in the above-quoted paragraph (see Fig. 1, for example). Thus, the Okita patent does not disclose or suggest the use of a Berlekamp-Massey module as is presently claimed. Furthermore, it is respectfully submitted that the Cameron patent does not disclose or suggest this type of Berlekamp-Massey module.

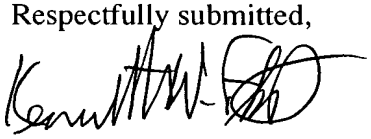
Contrary to the Examiner's arguments regarding Claim 4, for example, it is respectfully submitted that there is no teaching or suggestion contained in the cited patents that provide for a Berlekamp-Massey module comprising quadratic-subfield multipliers. The Examiner's unsupported assertion is mere conjecture as to what one or ordinary skill in the art would do. Absent some specific teaching or suggestion, it is respectfully submitted that the Examiner's position is unsupportable, or at best supportable only using hindsight reconstruction in light of Applicants' teachings.

Therefore, it is respectfully submitted that Claim 20 is not obvious in view of any of the cited patents, taken singly or together. Allowance of Claim 20 is respectfully requested.

The prior art made of record and not relied upon is considered pertinent to Applicants' disclosure to the extent indicated by the Examiner.

In view of the above, it is respectfully submitted that all pending Claims are allowable over the art of record and that this application is in condition for allowance. Reconsideration of this application and allowance thereof are earnestly solicited.

Respectfully submitted,



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